Cyclic Redundancy Check

The pattern is usually given in the form of a polynomial and can be implemented in hardware.

The frame check sequence (FCS) and the register size will always be less 1 less than the number of bits in the pattern.

There is only an XOR gate in front when the bit corresponding to the flip-flop has a value of 1.

Midterm Topics

Nyquist Theorem
Shannon Capacity Theorem
Data Encoding Techniques
    NRZI
Digital Data to Analog Signals
    QAM – phase angles and amplitudes
    In order to get 128 levels from analog modem, vary phase angle and amplitude
Stop-and-Wait Protocol
Utilization of media
Propagation delays
Time per frame
How many frames will fit on a link
Sliding window
Error Control
    Go back N
    Selective reject

Note sheet – 3x5 card size