Memory Control Signals

Memories in general have three control signals. They are usually active at 0 volts, as the ground signal is more stable than the power source general. If you run 5V on a wire, it generally decays to 4 or 3. If you rely on a 5V signal, you have to allow for a margin of error. Using 0V is more stable and does not have this need for a large margin of error.

The three signals historically found on memory chips:

- **CS – Chip select –** Provides the ability to select one chip over the other, based on the address being written to
- **OE – Output enable -** Disable outputs from driving voltage onto the wires
- **WR – Write -** Determines whether reading or writing to the memory

If power is retained, we effectively have always-on memory.

The memory chip used in lab can consume up to 1W of power.

If battery voltage drops below 4.25V, it's time to buy new batteries.

The key here is: if the DBUS is attached to any other memory chip or other circuit, it is important to bring the CS chip to high impedance when not communicating with it. Leaving it set to low results in interference patterns.

Communication between Controller and Memory

In the Motorola view of time, the clock period begins low and ends high.

A **synchronous memory** access requires that the memory be able to keep up with the microcontroller. It will give it a fixed amount of time to respond. The memory must be fast enough to meet the timing requirements of the controller.
Example: Motorola 68000

In an **asynchronous memory read**, the memory is allowed to hold up the controller.
Example: Motorola 68332

Read from Memory

Think of a memory cycle like text messaging.

In the case of a read cycle, it's like receiving a text message.

The first half of the E clock period is known as the addressing phase. It is in this time period that the controller sends the memory address to the memory chip. The second half of the E clock period is known as the **Data Phase**, in which the data is sent.

1. The HC11 does not hold a complete address through the cycle.

2. The HC11 drives voltage on A7:A0 during the address phase. Therefore, memory cannot.

A register is a single storage location and it has a clock edge which it uses to take a sample. It is a memory for the memory address.

Transparent trigger (HC373) -

OE - Output Enable
LE - Load Enable

When load is high, whatever is on D is being *continuously* sampled and moved to Q. This differs from the edge-triggered, in which samples only occur on an edge.

The *transparent* is used to describe the continuous sample

Load Enable is attached directly to memory strobe.