Our Memory Chip
Our memory chip is the 62256 and contains 32k.

Control Signals on the 62256
Command the chip to behave in a certain way.

Output enable – determines whether output circuitry is connected. A high disables output.
Write Enable – high is used to designate read and low is used to denote write.

During the addressing phase, the memory outputs must be disabled (in High-Z).
In the data phase, the memory outputs can be either enabled or disabled, depending on whether reading or writing is occurring.

The memory should only be active when E is high.

	CS	OE	WR
Read Cycle	0	0	1
Write Cycle	0	1	0

The HC11's RW pin is connected directly to the memory chip's WR signal.

Address Mapping
We need to map the 62256's 0x0000 – 7fff memory addresses into the HC11's memory space.

MC68HC11 Addresses
Min: 0x0000
Max: 0xffff

62256 Addresses
Min: 0x0000
Max: 0x7fff

The memory chip is mapped into the HC11's 0x8000 to 0xffff range.

The map bits should stay constant.