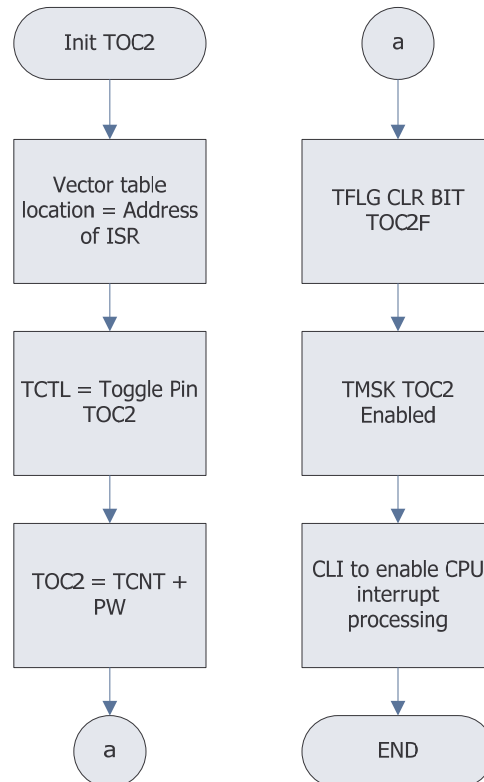


Initializing the TOC Behavior

Remember the standard steps:

1. Control registers
2. Parameters
3. Initial flag clear because time has started
4. Mask clear to enable the interrupts

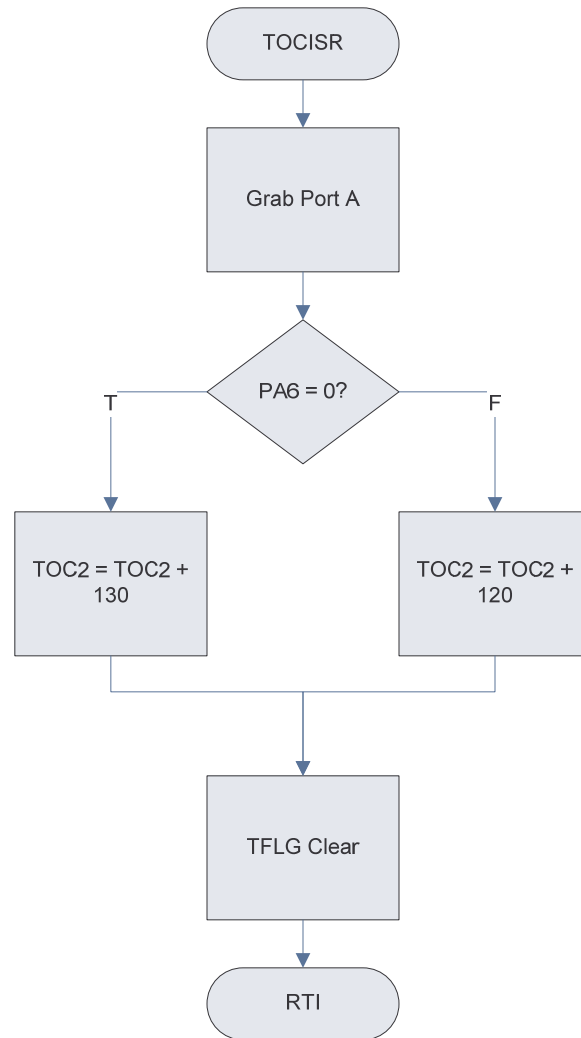
The Sequence



The timer has the ability to write voltages onto the pins for us.

The CPU has the ability to ignore interrupts, much like Dr. Meier could sit in his office, shut the door, and put his headphones on.

The control bits that allow the interrupt to be generated by the timer are in the mask registers. You cannot clear TFLG using BSET or BCLR. **You must do a LOAD-STORE pattern.** The reason there is a restriction on how you interact with the flag registers is to prevent programmers from clearing out and acknowledging all interrupts handled by the flag register. It is deliberately designed with a structure that makes you think about how you have to acknowledge the interrupt.



The Code

```

INIT:      LDS     #$DFFF
           LDX     #TOC2ISR      ; init special test TOC2 vector
           STX     0xBFE6

           ; Configure to toggle the signal
           LDAA   TCTL2
           ORAA   #%01000000
           ANDA   #%01111111
           STAA   TCTL2

           ; An alternate method of the above:
           ; -snip-
           LDX   #TCTL2
           BCLR  0,x %10000000
           BSET  0,x %01000000
           ; -snip-

           ; Drive TOC2 to 5V
           LDAA  PORTA
           ORAA  #%01000000
           STAA  PORTA
  
```

```
        ; Set the time of the interrupt
        LDD     TCNT
        ADDD    #120
        STD     TOC2

        ; Clear the interrupt flag
        LDAA   #%01000000      ; Write 1 to clear protection strategy
        STAA   TFLG1

        ; Enable the interrupt
        LDAA   TMSK1
        ORAA   #%01000000
        STAA   TMSK1

        ; Enable Interrupts
        CLI

TOC2ISR:    ...
           ...

           LDAA   PORTA
           ANDA   #%01000000
           BEQ    PINWENTLOW

           ...
           ...
           RTI
```